REMARKS

I. Introduction

In response to the pending rejection, Applicants have amended claims 1, 7, 14, 20, 26 and 33 so as to more clearly recite the intended subject matter of the present invention. In addition, new claims 45-50 have been added. New claims 45-50 recite additional aspects of the present invention not previously claimed. No new matter has been added.

Applicants respectfully submit that the pending claims are patentable over the cited prior art references for the reasons set forth below.

II. The Rejection Of Claims 1, 3, 5, 6, 20, 22, 24 And 25 Under 35 U.S.C. § 103

Claims 1, 3, 5, 6, 20, 22, 24 and 25 were rejected under 35 U.S.C. § 103 as being obvious over JP 05-024976 to Nakagawa, USP No. 4,596,645 to Stirn and USP No. 5,672,541 to Booske in view of Wolf, Silicon Processing for the VLSI Era. Applicants respectfully traverse this rejection for the following reasons.

As recited by each of the pending independent claims noted in the foregoing rejection, according to the present invention, during the generation of plasma, the impurity solid and the semiconductor substrate are in a state where no voltage is being applied thereto. Thereafter, during the mixing of the impurity into the plasma, the first voltage is applied to the impurity solid while the semiconductor substrate is maintained in a state where no voltage is being applied thereto. Further, during the introduction of the plasma, in which the impurity is mixed, to the semiconductor substrate, the second voltage is applied the semiconductor substrate held in the vacuum chamber after

resuming the impurity solid back to a state where no voltage is being applied thereto. Thus, voltages applied to the impurity solid and the semiconductor substrate are being switched in the foregoing manner during the process of the present invention.

Turning to the cited prior art references, Nakagawa discloses that the power source 108 is connected to the cathode 104, and the target 109 (corresponding to the impurity solid of the present invention) is provided on the cathode 104. Further, the test sample 105 (corresponding to the semiconductor substrate of the present invention) is provided in the anode 103, and plasma 107 is generated between the test sample 105 and the target 109. It is noted that a translation of the relevant portions of Nakagawa is provided herewith.

However, according to paragraph [0021] of Nakagawa, since the power source 108 is in an ON state during the generation of plasma 107, the target 109 is in a state where voltage is being applied thereto. In contrast, as set forth above, in the present invention, no voltage is being applied to the impurity solid during the generation of plasma. Thus, Nakagawa fails to disclose or suggest this element of claim 1.

In addition, according to paragraph [0021] of Nakagawa, since the test sample is withdrawn from the chamber 100 seconds after plasma 107 is generated, it would appear that after plasma 107 is generated, impurities are diffused from the target 109 to the test sample 105 through plasma 107. However, according to the present invention, after plasma is generated, the first voltage is applied to the impurity solid while the semiconductor substrate is maintained in a state where no voltage is being applied thereto, in order to mix the impurity into the plasma. Thereafter, the second voltage is applied the semiconductor substrate held in the vacuum chamber after resuming the

impurity solid back to a state where no voltage is being applied thereto, in order to introduce the plasma, in which the impurity is mixed, to the semiconductor substrate. Thus, Nakagawa also fails to disclose this element of claim 1.

Moreover, according to new claims 45-50, the semiconductor substrate is connected to the power supply via a switch, and the switch is switched ON or OFF according to the process as set forth above. However, in contrast, Nakagawa fails to disclose or suggest that a power supply is connected to the anode 103 in which the test sample 105 is provided via a switch, and that the switch functions to switch the power supply ON and OFF according to each step.

Turning to Stirn, referring to Fig. 2, this reference discloses a power source 36, 41 (see, Fig. 2), but fails to disclose that a switch is provided between the power source 36, 41 and the target or/and the substrate 40a. More importantly, Stirn does not appear to disclose or suggest that the voltages are applied during the process in the manner set forth in the amended claims. As such, Stirn also appears to fail to disclose or suggest the present invention as recited by the amended claims.

Turning to Booske, as noted in Applicants' previous response, this reference does not appear to disclose applying any type of voltage to the impurity solid. As set forth on col. 9, lines 14-21, Booske discloses firing ions at the target 46 (i.e., impurity solid) by means of an ion source 44 in order to sputter the target material and form the thin layer 38.this reference. As such, at a minimum, it is clear that Booske fails to cure the defects of Nakagawa and Stirn as related to claims 1 and 20.

Finally, it is noted that Wolf also appears to cure the defects of the foregoing three prior art references.

Accordingly, as each and every claim limitation must be disclosed or suggested by the cited prior art references in order to substantiate a rejection under 35 U.S.C. § 103 (*see*, M.P.E.P. § 2143.03), and the foregoing makes clear that the cited prior art references fail to do so, it is submitted that claims 1 and 20 are patentable over Nakagawa, Stirn, Booske and Wolf, taken alone or in combination with one another.

III. The Rejection Of Claims 7, 9, 11-13, 26, 28 And 30-32 Under 35 U.S.C. § 103

Claims 7, 9, 11-13, 26, 28 and 30-32 were rejected under 35 U.S.C. § 103 as being obvious over JP 5-024976 to Nakagawa and USP No. 5,672,541 to Booske in view of Wolf, Silicon Processing for the VLSI Era. Applicants respectfully traverse this rejection for the following reasons.

First, claims 7 and 26, which are the only independent claims in the foregoing rejection, recite the same elements as claims 1 and 20 discussed above in Section II. Accordingly, for the same reasons as set forth above in Section II, it is respectfully submitted that claims 7 and 26 are patentable over the foregoing references for at least the same reasons as noted above.

IV. The Rejection Of Claims 14, 16, 18, 19, 33, 35, 37 And 38 Under 35 U.S.C. § 103

Claims 14, 16, 18, 19, 33, 35, 37 and 38 were rejected under 35 U.S.C. § 103 as being obvious over JP 5-024976 to Nakagawa, USP No. 4,596,645 to Stirn and USP No. 5,672,541 to Booske in view of Wolf, Silicon Processing for the VLSI Era. Applicants respectfully traverse this rejection for the following reasons.

Claims 14 and 37, which are the only independent claims in the foregoing rejection, recite the same elements as claims 1 and 20 discussed above in Section II. Accordingly, for the same reasons as set forth above in Section II, it is respectfully submitted that claims 14 and 37 are patentable over the foregoing references for at least the same reasons as noted above.

V. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as all pending independent claims are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

VI. Conclusion

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 8/2/03

By: _____

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W., Suite 1200
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087

WDC99 729345-1.060188.0063

English Translation of

LAID OPEN unexamined

JAPANESE PATENT APPLICATION

Publication No. 5-024976A

[0018]

[Operation] FIG. 1 is a schematic view showing a construction of a doping system according to an embodiment of the present invention which is suitable for performing the doping method of the present invention.

[0019] A pair of electrodes of an anode 103 and a cathode 104 are provided in a chamber 101, which is capable of being evacuated by a vacuum pump 102. A sample 105 is set on the anode 103.

[0020] As the sample, a monocrystal or polycrystal semiconductor wafer or a polycrystal or amorphous semiconductor thin film deposited on a substrate of glass, metal or the like is used. These semiconductors may be or may not be doped beforehand according to the purpose. The sample 105 can be heated to a desired temperature by a heater 106. The cathode 104 is connected with a power source 108 for generating plasma 107 between the anode 103 and the cathode 104. A target 109 is set on the cathode 104. As a material of the target, B, Al, Ga, In, Tl, P, As, Sb, Bi or the like is used. The power source 108 may be a DC power source or a high frequency power source. Particularly, when using a target of which material has a high resistance, a power source having a radiofrequency at, for example, 13.56 MHz or the like can be sued suitably. An inert gas such as Ar is introduced from a bombe into the chamber 101. The flow rate of the inert gas is adjusted by a mass flow controller 111. The pressure inside the chamber 101 is adjusted by respective openings of the mass flow controller 111 and a butterfly valve 114. Mercury lamps 112, 113 (hereinafter referred to as light sources 112, 113) are provided as UV light sources within the chamber 101 so as to inrradiate the surface of the sample as needed.

[0021] EXPERIMENT 1

The following experiment was conducted for confirming the effects of the present invention. As the sample 105, a p-type Si wafer (resistivity: 1 ohm·cm) having a sintered metal electrode on the reverse side thereof was set in the doping system in FIG. 1. After the pressure inside the chamber 101 was reduced by evacuation to 10^{-6} Torr, Al of 5 sccm was flown and the butterfly valve 114 was adjusted to set the pressure 10^{-3} Torr. Then, the electric current to the heater 106 was adjusted so as to set the temperature of the substrate 100°C. A plate of simple substance of P having purity of 99.9% was used as the target 109. Next, the light sources 112, 113 were operated. When high frequency power of 200 W was supplied from the power source 108 under the above state, while adjusting a matching circuit (not shown) so as to allow the reflection power to be the minimum, plasma 107 was generated. After 100 seconds passed under this state, power supply to the power source 108, the light sources 112, 113 and the heater 106 was stopped. After being cooled, the sample was taken out from the chamber 101 and cut into 1 cm squares to obtain a sample 1A.

[0022] Next, for comparison, a sample 1B was obtained by the same method as above, only with a difference that the light sources 112, 113 were not operated.

[0023] Next, a conductor was fixed to the reverse surface and the obverse surface of each of the samples 1A, 1B by means of silver paste. First, the voltage/current characteristic was measured for each sample in the dark place. The sample 1A had the rectification ratio of 3×10^4 times at 1V, while the sample 1B had that of 50 times only. Further, the solar battery characteristic was measured for each sample by a solar simulator with the air mass (AM) of 1.5. The sample 1A had the conversion efficiency (η) of 9.3 %, which exhibited an excellent characteristic as a slower battery with no reflection film. On the other hand, the sample 1B had the conversion efficiency (η) of 2.7 %, which was insufficient for a solar battery.

[0042]

[EMBODIMENTS] The method and apparatus for processing the surface of a semiconductor according to the embodiments will be hereinafter described for explaining the present invention, wherein the present invention is not limited to by the description.

[0043] Embodiment 1

In the present embodiment, a pin-type a-Si photoelectromotive element 408 having the structure shown in the schematic section of FIG. 4 is fabricated by using the system shown in FIG. 1. This pohotoelectromotive element 408 is a photoelectromotive element fabricated by depositing and forming, on a substrate 401 in this order, a lower electrode 402, a n-type semiconductor layer 403, an i-type semiconductor layer 404, a p-type semiconductor layer 405, a transparent electrode 406 and a collector electrode 407. Wherein, the pohotoelectromotive element 408 in this embodiment is premised that light is made incident from the transparent electrode 406 side.

[0044] First, a stainless square substrate (5 cm × 5 cm) is set in a commercially available sputtering system (SBH-2206DE produced by ULVAC, Inc.), and then, sputtering is performed to deposit an Ag thin film of 0.3 μm, using Ag (99.99%) as a target and subsequently to deposit a ZnO thin film of 1.5 μm, using ZnO (99.9%) as a target, thereby forming the lower electrode 402.

[0045] Subsequently, the substrate on which the lower electrode 402 is formed is set in a commercially available plasma CVD system (CHJ-3030 produced by ULVAC, Inc.). Rough vacuum evacuation and high vacuum evacuation are repeated by the exhaust pump through the exhaust pipe of the reaction vessel. At this time, the temperature control mechanism controls the surface temperature of the substrate to be 250 °C.

[0046] After sufficient evacuation, SiH_4 of 300 sccm, SiF_4 of 4 sccm, PH_3/H_2 (H_2 of 1 % diluted) of 55 sccm and H_2 of 40 sccm are introduced through the gas introduction pipe and the opening of the throttle valve is adjusted to maintain the pressure inside the reaction vessel to be 1 Torr. Immediately after the pressure is

stabilized electric power of 200 W is applied by the high frequency power source. Generated plasma is kept for 5 minutes. Thus, a n^+ a-Si:H:F film as a n^+ semiconductor layer 403 is formed on the lower electrode 402.

[0047] After re-evacuation, SiH_4 of 300 sccm, SiF_4 of 4 sccm, H_2 of 40 sccm are introduced next through the gas introduction pipe and the opening of the throttle valve is adjusted to maintain the pressure inside the reaction vessel to be 1 Torr. Immediately after the pressure is stabilized, electric power of 150 W is applied by the frequency power source. Geneated plasma is kept for 40 minutes. Thus, an a-Si:H:F film as the i-type semiconductor layer 404 is formed on the n-type semiconductor layer 403.

[0048] Next, the substrate 401 is taken out from the plasma CVD system and is set into the doping system shown in FIG. 1. Electric discharge is continued for 70 seconds with the use of boron (B) as a target, while irradiating UV light under the conditions of the flow rate of Ar of 5 sccm, the pressure of 2×10^{-3} Torr, the substrate temperature of 100 °C and discharge electric power of 200 W, thereby a p-type semiconductor layer 405 is formed on the i-type semiconductor layer 404.

[0049] Next, the transparent electrode 406 (ITO (In_2O_3+SnO_2) is formed by vacuum deposition, and a collector electrode 407 (Al) is mask-deposited. Thus, the pohtoelectromotive element 408 is completed.

[0050] The characteristic of the thus fabricated photoelectromotive element 408 is evaluated under light irradiation with the air mass (hereinafter referred to as AM) of 1.5 (100 mW/cm^2), to obtain the photoelectric conversion efficiency (η) of 9.3 %. Further, after continuation of light irradiation with AM of 1.5 (100 mW/cm^2) for 500 hours, the change ratio of the photoelectric conversion efficiency with respect to the initial value is measured to find that the change ratio falls within 20 %.